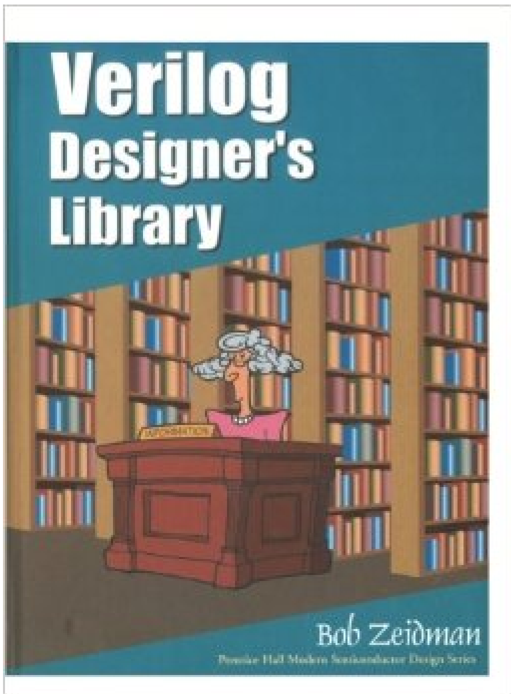
Verilog Designer's Library



Synopsis

Ready-to-use building blocks for integrated circuit design. Why start coding from scratch when you can work from this library of pre-tested routines, created by an HDL expert? There are plenty of introductory texts to describe the basics of Verilog, but Verilog Designer's Library is the only book that offers real, reusable routines that you can put to work right away.   Verilog Designer's Library organizes Verilog routines according to functionality, making it easy to locate the material you need. Each function is described by a behavioral model to use for simulation, followed by the RTL code you'll use to synthesize the gate-level implementation. Extensive test code is included for each function, to assist you with your own verification efforts. Coverage includes: Essential Verilog coding techniques Basic building blocks of successful routines State machines and memories Practical debugging guidelines   Although Verilog Designer's Library assumes a basic familiarity with Verilog structure and syntax, it does not require a background in programming. Beginners can work through the book in sequence to develop their skills, while experienced Verilog users can go directly to the routines they need. Hardware designers, systems analysts, VARs, OEMs, software developers, and system integrators will find it an ideal sourcebook on all aspects of Verilog development.

Book Information

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Customer Reviews

I am a senior systems engineer. This book has been instrumental in getting some of our new engineers quickly up to speed in Verilog so that they could begin doing design right away. This book doesn’t try to solve every problem because it doesn’t have to - instead it enables the reader to learn the cornerstones of design, teaching the user necessary skills and not simply cookbook repetitions. Synthesizable code is treated more fairly in this text than others. I was very pleased to add this to my library.

I was looking for models for a dual-port RAM and a FIFO. I couldn’t find any book that had examples of either one of them. This book does and in great detail. That was worth the price of the book for me.

This book is good for beginners, it has a few good ideas in it. The Behavioral vs. RTL versions of the code is pretty useless, but the RTL vs. Simulation versions are useful. Getting a quick and dirty unit test bench up and running is a good idea. But DO NOT USE THE ASYNCHRONOUS FIFO. It does not work. If you are crossing clock boundaries, this is not the way to do it!

This is a bad book, overall. I just pick 3 exemplary issues:.) The distinction between behavioural and RTL code in the examples is only there to double the number of pages. The listings are essentially the same, they differ in typically, like, 5 lines. Moreover, most synthesis tools would accept both programs and create the same circuit..) creating Verilog code from 3 pages of C which could be done in 10 lines of Perl is not really state of the art..) Worst of all: The asynchronous fifo does not protect the pointers on the clock domain boundary, so it is unusable in the real world.Either Bob Zeidman is not really up to date with his Verilog design skills, or it’s the Dogbert priciple of "Beware the advice of successful people; they do not seek company."

With many verilog books out there, this one has to be the best I’ve seen. It has real world modules, and explains what went into each module. This book is a MUST for any Beginner->Advanced ASIC designer. Highly recommended!!

I am a power user of Verilog. I have "all" the books on Verilog. I bought this book just to make sure that my library is complete. Atleast 1/3rd of this book is complete waste. Who writes behavioral code for counters and adders? Behavioral code section for all the modules is unnecessary. Author should remove them and save paper (save trees too). Behavioral code is used in real life to simulate parts of design which can not be described in RTL like memories or some processor macros and not to describe simple designs.A real life designer will never keep such simple models in his library. Most models are suitable as a starting guide for a beginner. I think book should be renamed as "Verilog Beginner’s Library"BTW I will surely congratulate author for collecting many different kinds of models in one place. I give 2 stars for this effort.

I have several Verilog texts in my library, and I refer to this one quite often. The examples are clear and concise and compile without error direct from the included CD. People looking to this text to "lift" code and drop into their design will probably have issues, but this is standard faire in the design world. Hardly is code directly ported to the next design.Bob was also helpful in quickly replying to emails when I have questions

Tired of reinventing the wheel? Complete designs are provided for basic building blocks such as FIFOs, RAM controller, dual port RAM, State machines, etc. This book has proven an indispensable starting point.